AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph [0005] with the following paragraph rewritten in amendment format:

[0005] In U.S. Patent No. 6,077,303 to Mandell et al. and [[my]] co-pending application "Application Specific Integrated Circuit Design Tool and File Structure" ~~"Architectural Structure Of A Process Netlist Design Tool"~~, Serial No. 09/918,596 [[_____]], filed July 31, 2001[[_____]] , and assigned to The Boeing Company, a design tool and method for simplifying the design of ASICs is disclosed. The design tool and method generates symbolic and numeric equations. In situations involving relatively less complex, small to medium ASICs, the symbolic equations that are generated by the design tool are finite and computationally feasible. In other words, the symbolic equations require a limited amount of computer storage and running time to be further simplified. However, when more complex circuits are involved (such as large ASICs and/or circuits including cascaded finite impulse response (FIR) filters, closed-loops, and other complex components), the resulting set of symbolic equations become large enough to overflow the memory that is available to the workstation and/or the capability of the symbolic manipulation tool that is used to compare the equations.